AK

Notice of Allowability	Application No.	Applicant(s)	
	10/666,507	KIM ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 22 December 2004*.

2. ☒ The allowed claim(s) is/are *1-6 and 16*.

3. ☒ The drawings filed on *19 September 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

This office action is in response the filing of the amendment filed on 22 December 2204. Claims 1-6 and 16 are pending; claims 7-15 have been cancelled.

Allowable Subject Matter

Claims 1-6 and 16 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest a MOS transistor where an isolation layer is formed at a predetermined region of a semiconductor substrate to define an active region; an upper trench region formed in the active region, the upper trench region crossing the active region to divide the active region into two sub-active regions; a spacer covering al least a pair of sidewalls of the upper trench region that are adjacent to the active region; a lower trench region formed under the upper trench region surrounded by the spacer; a pair of a low concentration source/drain region formed under the spacer, the low concentration source/drain regions being shallower than the lower trench region; a pair of high concentration source/drain regions formed at top surfaces of the sub-active regions that are located at both sides of the upper trench region respectively; a gate insulating layer covering the sidewalls and a bottom surface of the lower trench region; and a gate electrode filling the lower trench region surrounded by the gate insulating layer and filling the upper trench region, surrounded by the spacer.

For example, Tseng (6,358,800) discloses a MOS transistor where an isolation layer formed at a predetermined region of a semiconductor substrate to define an active region; an upper trench region formed in the active region, the upper trench region crossing the active region to divide the active region into two sub-active regions; a spacer covering at least a pair of sidewalls of the upper trench region that are adjacent to the active region; a lower trench region formed under the upper trench region surrounded by the spacer; a pair of high concentration source/drain regions formed at top surfaces of the sub-active regions that are located at both sides of the upper trench region respectively; a gate insulating layer covering a bottom surface of the lower trench region; and a gate electrode filling the lower trench region, and filling the upper trench region, surrounded by the spacer. Tseng further discloses the spacer comprising a first spacer adjacent to the active region and a second spacer adjacent to the isolation layer, the first spacer having the same width as the second spacer. Tseng also discloses a pair of low concentration source/drain regions formed in the semiconductor substrate under the first spacer, and formed in contact with sidewalls of the lower trench region.

However, Tseng does not disclose, anticipate, teach, or suggest a pair of a low concentration source/drain region formed under the spacer, the low concentration source/drain regions being shallower than the lower trench region.

Sugawara et al. (6,171,916) disclose a MOS transistor where an isolation layer formed at a predetermined region of a semiconductor substrate to define an active region; a trench region formed in the active region, the trench region crossing the active region to divide the active region into two sub-active regions; a pair of high

concentration source/drain regions formed at top surfaces of the sub-active regions that are located at both sides of the trench region respectively; a gate insulating layer covering the sidewalls and a bottom surface of the trench region; and a gate electrode filling the trench region, surrounded by the gate insulating layer. However, Sugawara et al. do not disclose, anticipate, teach or suggest a pair of a low concentration source/drain region formed under the spacer, the low concentration source/drain regions being shallower than the lower trench region.

The prior art made of record in this action does not anticipate, teach, or suggest a MOS transistor where an isolation layer is formed at a predetermined region of a semiconductor substrate to define an active region; an upper trench region formed in the active region, the upper trench region crossing the active region to divide the active region into two sub-active regions; a spacer covering al least a pair of sidewalls of the upper trench region that are adjacent to the active region; a lower trench region formed under the upper trench region surrounded by the spacer; a pair of a low concentration source/drain region formed under the spacer, the low concentration source/drain regions being shallower than the lower trench region; a pair of high concentration source/drain regions formed at top surfaces of the sub-active regions that are located at both sides of the upper trench region respectively; a gate insulating layer covering the sidewalls and a bottom surface of the lower trench region; and a gate electrode filling the lower trench region surrounded by the gate insulating layer and filling the upper trench region, surrounded by the spacer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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